REMARKS

The Office Action dated August 9, 2006 has been received and carefully noted. The above noted amendments to the claims, and the following remarks, are submitted as a full and complete response thereto. Claims 21-25 have been cancelled from consideration and new claims 36-40 have been added to the application. No new matter has been introduced, and therefore, claims 1-20 and 26-40 are pending and submitted for consideration.

Claim 17 was objected to in the Office Action for an informality in line 3. Applicants have addressed the formality in the above noted amendment to claim 17, and therefore, reconsideration and withdrawal of the objection is respectfully requested.

Claims 21-25 were rejected under 35 USC §101 are being directed to non-statutory subject matter. Applicants have cancelled claims 21-25, and therefore, Applicants submit that the rejection is moot. Further, Applicants have submitted new claims 36-40, which as also directed to a computer program embodied on a computer readable medium. However, each of these claims recites that the program operates to control a method, which Applicants submit clearly constitutes statutory subject matter. Therefore, withdrawal of the rejection of claims 21-25 and favorable consideration of new claims 36-40 is respectfully requested.

Claims 1, 2, 7, 8, 13-19, and 21-25 stand rejected under 35 U.S.C. §103(a) as being obvious in view of *Muller* (US Patent No. 6,453,360) in view of *Steiss* (US Patent No. 6,895,494). The Office Action took the position that *Muller*

teaches each and every element recited in claims 1, 2, 7, 8, 13-19, and 21-25, except for processing the plurality of instruction fields in parallel. However, the Office Action cites to *Steiss* as teaching this feature, and as such, the Office Action concluded that it would have been obvious to one of ordinary skill in the art to have combined the teaching of the references to generate Applicants' claimed invention. Applicants traverse the rejection and respectfully submit that the cited combination of references, when taken alone or in combination, fails to teach, show, or suggest each and every limitation recited in claims 1, 2, 7, 8, 13-19, and 21-25.

Claim 1, upon which claims 2-6 directly or indirectly depend, recites a method for a programmable micro-controller. The method includes loading an instruction word within the micro-controller, the instruction word having a plurality of instruction fields, and processing the plurality of instruction fields in parallel, each instruction field related to a specific operation for parsing a packet or encapsulating data to form a packet.

Claim 7, upon which claims 8-15 directly or indirectly depend, recites a programmable micro-controller. The micro-controller includes an embedded memory to store one or more instruction words, each instruction word including a plurality of instruction fields, and one or more processing engines, each processing engine to process the plurality of instruction fields in parallel for each instruction word, each instruction field related to a specific operation for parsing a packet or encapsulating data to form a packet.

Claim 16, upon which claims 17-20 directly or indirectly depend, recites a programmable micro-controller comprising an embedded buffer memory a register set, and programmable processing circuitry coupled to the embedded buffer memory and the register set, the programmable processing circuitry including a plurality of execution units, each execution unit to execute in parallel an operation within an instruction using the register set, the processing circuitry to parse a packet in the embedded buffer memory for extract data or to encapsulate data in the embedded buffer memory to form a packet using the execution units.

Claim 26, upon which claims 27-30 directly or indirectly depend, recites a template within a system on a chip. The template includes a plurality of calls to routines, each routine associated with a particular protocol. Each routine includes one or more instructions, and each instruction includes a plurality of operation fields that are processed in parallel to parse a packet or to encapsulate data to form a packet.

However, Applicants submit that the cited combination of references, when taken alone or in combination, fails to teach, show, or suggest each and every element recited in claims 1, 2, 7, 8, 13-19, and 21-25. More particularly, *Muller* teaches a network interface for receiving a packet from a network and transferring the packet to a host computer system. A header portion of the received packet is parsed by a parser module to determine the packet's compatibility or conformance with pre-selected protocols. If the packet is determined to be compatible, a number of processing functions are performed to increase the efficiency with

which the packet is handled. In one function, a re-assembly engine re-assembles, in a re-assembly buffer, data portions of multiple packets in a single communication flow or connection. Header portions of these packets are stored in a header buffer. In another function, a packet batching module determines when multiple packets in one flow are transferred to the host computer system, so that their header portions are processed collectively rather than being interspersed with headers of other flows' packets. In another function, the processing of packets through their protocol stacks is distributed among multiple processors by a load distributor, based on their communication flows.

In *Muller*, a flow database is maintained by a flow database manager to reflect the creation, termination, and activity of flows. A packet queue stores packets to await transfer to the host computer system, and a control queue stores information concerning the waiting packets. If the packet queue becomes saturated with packets, a random packet may be discarded. An interrupt modulator may modulate the rate at which interrupts associated with packet arrival events are issued to the host computer system. However, as noted in the Office Action, *Muller* does not teach, show, or suggest any sort of parallel processing of instruction fields.

Steiss teaches a sub-pipelined translation that provides binary compatibility between current and future generations of DSPs. In the disclosure of *Steiss*, when a fetch packet is retrieved from memory, the entire fetch packet is assigned an operating mode, which is a base instruction set or migrant instruction set,

according to the execution mode at the time the request was made to the instruction memory for the fetch packet. The fetch packets from the instruction memory are parsed into execute packets and sorted by execution unit in a data path shared by both execution modes. Since the fetch packet syntax and execution unit encoding is different between the migrant and base architecture in this case, the two execution modes have separate control logic. Instructions from the dispatch data path are decoded by either base architecture decode logic or the migrant architecture decode logic, depending on the execution mode bound to the parent fetch packet of the instructions being decoded. Code processed by the migrant and base decode pipelines produces machine words that control the register files and the execution hardware functional units. These machine words are selected with a multiplexer, and the choice of the eventual machine word from the multiplexer is governed by the operating mode bound to the fetch packet that produced the machine word and sequencing logic for sub-pipelined execution. The selected machine word controls a global register file, which supplies operands to all hardware execution units and accepts results of all hardware execution units.

However, Applicants submit that neither *Muller* nor *Steiss* teaches, shows, or suggests processing instruction fields in parallel, when each instruction field is related to a specific operation for parsing a packet or encapsulating data to or from a packet, as recited in each of independent claims 1 and 7, and similarly recited in independent claims 16 and 26. The Office Action cites to column 1, line 11 through column 2, line 56 in *Steiss* as teaching parallel processing of instruction

fields; however, Applicants submit that the cited discussion in *Steiss* does not teach Applicants recited limitation of processing instruction fields in parallel, when each instruction field is related to a specific operation for parsing a packet or encapsulating data to or from a packet, as recited in the present claims. Rather, *Steiss* merely uses the phrase "instruction level parallelism," (*see,* column 2, lines 54-55) to represent the use of VLIW processors to issue multiple operations per cycle with simple control logic, which is not in any way synonymous with the recitation of parallel "processing" of instruction fields recited in Applicants' claims. Therefore, Applicants submit that the cited combination of references fails to teach, show, or suggest each and every limitation recited in claims 1-2, 7-8, 13-19, and 21-25. As such, reconsideration and withdrawal of the rejection of the claims is respectfully requested.

Additionally, Applicants submit that the cited combination of references, *e.g.*, *Muller* and *Steiss*, are not properly combinable in support of a rejection of claims 1-2, 7-8, 13-19, and 21-25 under 35 USC §103(a). More particularly, Applicants submit that it is well known that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention, where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves, or in the knowledge generally available to one of ordinary skill in the art. *See*, In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000).

In the instant case, the Office Action has merely stated that it would have been obvious to one of ordinary skill in the art to combine the references to increase efficiency, without citing to any particular section from either of the references that illustrates that one of ordinary skill in the art would have been motivated to combine the teaching of the references to increase the efficiency. Further, the Office Action has not presented any support for the conclusion that one of ordinary skill in the art would have known to combine the teaching of the references at the time the instant application was filed, other than to simply conclude that one would have known to do so to increase efficiency, without citation to any supporting documentation. Rather, the Office Action has merely drawn a broad conclusion that one of ordinary skill in the art could have combined the references to generate the claimed invention, despite the fact that *Steiss*' "parallelism" is directed to issuing multiple operations and Applicants' parallel processing is directed to "processing instruction fields."

In response to this broad unsupported conclusion, Applicants note that M.P.E.P. §2143.01 states that the mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art **also suggests the desirability** of the combination. See, In re Mills, 916 F.2d 680, 16 USPQ 2d 1430 (Fed. Cir. 1990). When the Office Action fails to provide specific motivation to combine references (more than a mere statement that it would have been obvious to combine the references), then the Federal Circuit, the Board, and the M.P.E.P are clearly aligned in taking the position that "the

references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention." See, M.P.E.P § 2141 and Hodosh v. Block Drug Co., Inc. 786 F.2d 1136, 229 USPQ 182 (Fed. Cir. 1986).

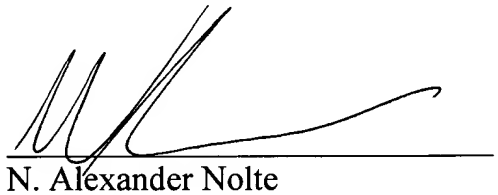
Applicants submit that the Office Action has not cited any support from within the references themselves that supports a conclusion that the references were combinable. Further, the Office Action has not provided any support for a conclusion that the motivation to combine the references was available to one of ordinary skill in the art at the time the present application was filed. As such, Applicants submit that the references supporting the §103 rejection are not properly combinable. In view of the improper combination of the cited references, reconsideration and withdrawal of the rejection of claims 1-2, 7-8, 13-19, and 21-25 under 35 USC §103(a) over *Muller* and *Steiss* is respectfully requested.

Therefore, in conclusion, Applicants submit that each of claims 1-2, 7-8, 13-19, and 21-25 recite subject matter that is not taught, shown, or otherwise suggested by the combination of *Muller* and *Steiss*. Additionally, Applicants submit that there is no motivation, either in the references themselves or in the knowledge available to one of ordinary skill in the art at the time the present application was filed, to combine the teaching of *Muller* and *Steiss*. Therefore, reconsideration and withdrawal of the rejection of claims 1-2, 7-8, 13-19, and 21-25 is respectfully requested.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



N. Alexander Nolte
Registration No. 45,689

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802

NAN:kzw